## REMARKS

Applicants respectfully request the Examiner's consideration of the present application as amended. Claims 1 and 14-32 remain in the application. Claims 1 and 21 have been amended.

The Examiner objects to claim 16, stating that "in to" should be "into." Applicants note that the correction requested by the Examiner was made in the Preliminary Amendment filed on August 23, 2002. Therefore, no amendment to claim 16 is necessary. Applicants therefore respectfully request the withdrawal of this objection.

Applicants respectfully submit that the claims are not anticipated by U.S. Pat. No. 5,361,373 of Gilson ("Gilson") and U.S. Pat. No. 5,668,815 of Gittinger et al. ("Gittinger").

Gilson discloses an integrated circuit computing device wherein:

> Host 40 reconfigures the FPGA 12 which causes new configuration data to be written into the Configuration Memory Array 20. Now referring to FIG. 2, the effect of this new configuration data is to . . . change the programming of the Logic Blocks 34 that comprise the Reconfigurable Instruction Execution Unit 16 such that the desired complex operation can be accomplished by the newly configured hardware on data that already exists within the Reconfigurable Instruction Execution Unit 16.

(Gilson Col. 7, lines 22-35).

Gilson discloses that host 40 reconfigures the FPGA 12 (col. 7 line 22). Gilson fails to teach or suggest a multi-master system bus that may be controlled for configuration using a first device, selected from among a group. Rather, Gilson discusses only a single master bus, with a single possible device, Host 40, which may configure the FPGA. Additionally, Gilson fails to disclose that FPGA 12 has a DMA controller with which to control the system bus for configuration.

Claim 1, as amended, on the other hand, recites:

> A method of using a multi-master system bus on a configurable system on a chip (CSoC), the CSoC including configurable system logic (CSL), the method comprising:
> controlling the multi-master system bus for configuration using a first device, the first device comprising a selectable one of an on-chip central processing unit (CPU), a direct memory access (DMA) controller, and an external control device;
> configuring a memory cell in the CSL using the multi-master system bus; and
> reading the memory cell in the CSL using the multi-master system bus.

(Claim 1, as amended). As noted above, Gilson does disclose a multi-master system bus, which may be controlled by one of multiple masters. Furthermore, Gilson does not disclose a DMA controller controlling a system bus for configuration. Therefore, claim 1, as amended, is not anticipated by Gilson. Claims 2-3 and 14-20 depend on claim 1, and incorporate its limitations. Therefore, for at least the same reasons advanced above with respect to claim 1, claims 14-20 are not anticipated by Gilson.

Gittinger states that a

> Microcontroller 10 includes a clock/power management unit 12, an interrupt control unit 14, a processor core 16, a timer control unit 18, a DMA control unit 20, a programmable input/output (PIO) unit 22, an asynchronous serial interface 24, a synchronous serial interface 26, a chip select unit 28, an internal memory 30, and a bus interface unit 32.

(Gittinger Col. 5, lines 19-26). The microcontroller of Gittinger does not include configurable a configurable system logic ("CSL"). Applicants respectfully submit that the internal memory 30 of Gittinger is not a configurable system logic. Internal memory is generally random access memory (RAM) or similar memory. This is distinct from configurable system logic, as claimed in the present invention. The Examiner states

that "configurable system logic" is taught by internal memory 30 of Gittinger, since memory 30 is configurable by virtue of being able to store data.

Applicants respectfully disagree of this interpretation of the term "configurable system logic." The term, as is known in the art, refers to programmable logic devices, such as FPLDs, which "are programmed to perform user-specified logic functions by loading configuration data into the FPLD." (Specification, Description of Related Art, pg. 1, lines 13-16.) Applicants respectfully submit that this well known definition, which is reiterated in the Specification, should be accepted for the term "configurable system logic." Clearly, memory does not qualify under this definition, since it cannot perform logic functions, based on configuration data. Applicants respectfully submit that the Examiner has shown no references, which define a memory as a "configurable system logic." Applicants respectfully submit, therefore, that the above definition should be accepted by the Examiner in accordance with MPEP 2173.05(a).

Claim 1, as amended, on the other hand, recites:

> A method of using a multi-master system bus on a configurable system on a chip (CSoC), the CSoC including configurable system logic (CSL), the method comprising:
> controlling the multi-master system bus for configuration using a first device, the first device comprising a selectable one of an on-chip central processing unit (CPU), a direct memory access (DMA) controller, and an external control device;
> configuring a memory cell in the CSL using the multi-master system bus; and
> reading the memory cell in the CSL using the multi-master system bus.

(Claim 1, as amended). As noted above, Gittinger does not disclose controlling a multi-master system bus for configuration of a CSL using a first device, selected from among a group. Gittinger does not disclose a multi-master system bus, since only one



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bus master is discussed. Furthermore, Gittinger does not disclose configuring a memory cell in a configurable system logic, as noted above. Therefore, claim 1, as amended, is not anticipated by Gittinger. Claims 2-3 and 14-20 depend on claim 1, and incorporate its limitations. Therefore, for at least the same reasons advanced above with respect to claim 1, claims 14-20 are not anticipated by Gittinger.

Claim 21 recites:

> A method of configuring a configurable system on a chip (CsoC) comprising:
> initiating configuration of the CsoC using an on-chip central processing unit (CPU);
> passing control of a multi-master system bus to a first device for configuring on-chip configurable system logic (CSL);
> configuring a memory cell in the CSL using the first device.

(Claim 21). Gittinger does not disclose passing control of a system bus to a first device for configuring a CSL. Rather, Gittinger states that a DMA may be used to test memory. However, a memory test of a RAM or similar internal memory is dissimilar from configuring a memory cell in a configurable system logic, as recited in claim 21. Furthermore, in Gittinger, the DMA does not become the bus master of a multi-master bus, but rather uses direct memory access to test the memory. Therefore, claim 21, and claims 22-29 which depend on it, are not anticipated by Gittinger.

Claim 30 recites:

> A method comprising:
> initiating configuration of a configurable system on chip (CsoC) using an on-chip central processing unit (CPU);
> configuring a memory cell in the CSL using a first device of a group of devices, the group of devices comprising the CPU, a direct memory access (DMA) controller, and an external control device;
> reading a memory cell in the CSL using a second device selected from the group of devices; and
> selecting a signal in the CSoC to determine if the system bus is used for configuration or general interconnect of the CSoC.

(Claim 30). As noted above, Gittinger does not disclose configuring a memory cell in a configurable system logic using a device selected from a group of devices.

Furthermore, Gittinger does not disclose selecting a signal to determine if the system bus is being used for configuration or general interconnect. The Examiner notes that Gittinger teaches the use of a PIO pin, which indicates whether the microcontroller is operating in a test mode of operation. However, this is not equivalent to, nor does the Examine explain how this could be equivalent to, selecting a signal to determine whether the system bus is being used for configuration of general interconnect. A microcontroller cannot be used for "general interconnect" and therefore clearly cannot have a signal selecting whether it is used for configuration or general interconnect. Therefore, Gittinger does not disclose selecting a signal to determine if the system bus is being used for configuration or general interconnect.

Therefore, claim 30, and claims 31 and 32 which depend on it, are not anticipated by Gittinger.

Applicants respectfully submit that in view of the amendments and discussion set forth herein, the applicable rejections have been overcome.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due and not covered by any check submitted.

Respectfully submitted,

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